SYNOPSYS®

A Quick Guide to University Software Program

Courseware, SolvNetPlus & Synopsys Learning Center

February 2024

CONTENT

About SARA

What is Synopsys Academic & Research Alliances (SARA) ?

Through innovative collaborations, shared programs, and access to advanced technologies, Synopsys Academic & Research Alliances (SARA) is dedicated to furthering university research and education in the field of electronic design.

By investing in science, technology, engineering, and mathematics (STEM) education, we aim to nurture the interests and skills that are needed to bring the next generation of engineers into the workforce and the research labs.

Website Link

Who we help

Student

Empower and educate the next generation of engineers to be ready to tackle the latest challenges, whether in research or in industry.

Educator

Provide learning opportunities and training materials while lowering the barriers to access Synopsys technology for education and research.

Researchers

Address the ever-evolving challenges of the semiconductor industry, uncover new solutions, and pave the path toward future technologies.

Entrepreneurs

Collaborate to discover new technologies and turn fresh ideas into market-ready products for our Smart Everything world.

University Software Program Membership Benefits

SolvNetPlus

A repository of self-help resources to resolve many support issues, provide access to training, and many educational materials.

Synopsys Learning Center

Synopsys Learning Center offers a wide range of courses **(short training, instructor led, quick tips)** in different delivery modes and allows easier navigation and a more personalized learning experience, all while using your SolvNetPlus credentials.

Curriculum

Semester-length course contains material including **syllabus, lectures, labs, homework, and exams.** Synopsys tools are applied in the labs for a thorough and practical understanding of theoretical concepts introduced in each course.

Libraries, PDKS, and Memory Compiler

Teaching resources are offered to ensure students gain valuable experience using a complete design flow and to master advanced design methods such as low power and analog/mixed signal.

Reference Methodology Retrieval System

RMgen provides an easy way to configure and download product-specific and release-specific reference methodology scripts. These scripts are a starting point for developing product-specific flow scripts. Customize the scripts to work in your design environment.

SolvNetPlus

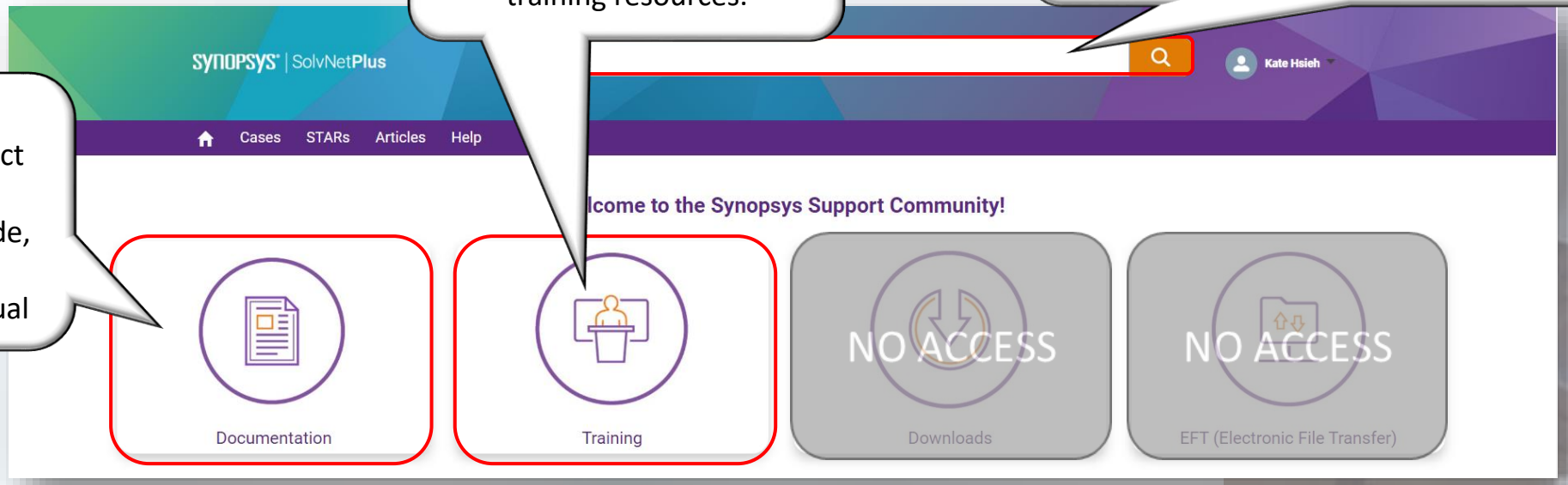
What is SolvNetPlus?

SolvNetPlus provides **Documentation, Training, and a comprehensive, searchable knowledge base** that provides solutions to frequently encountered problems.

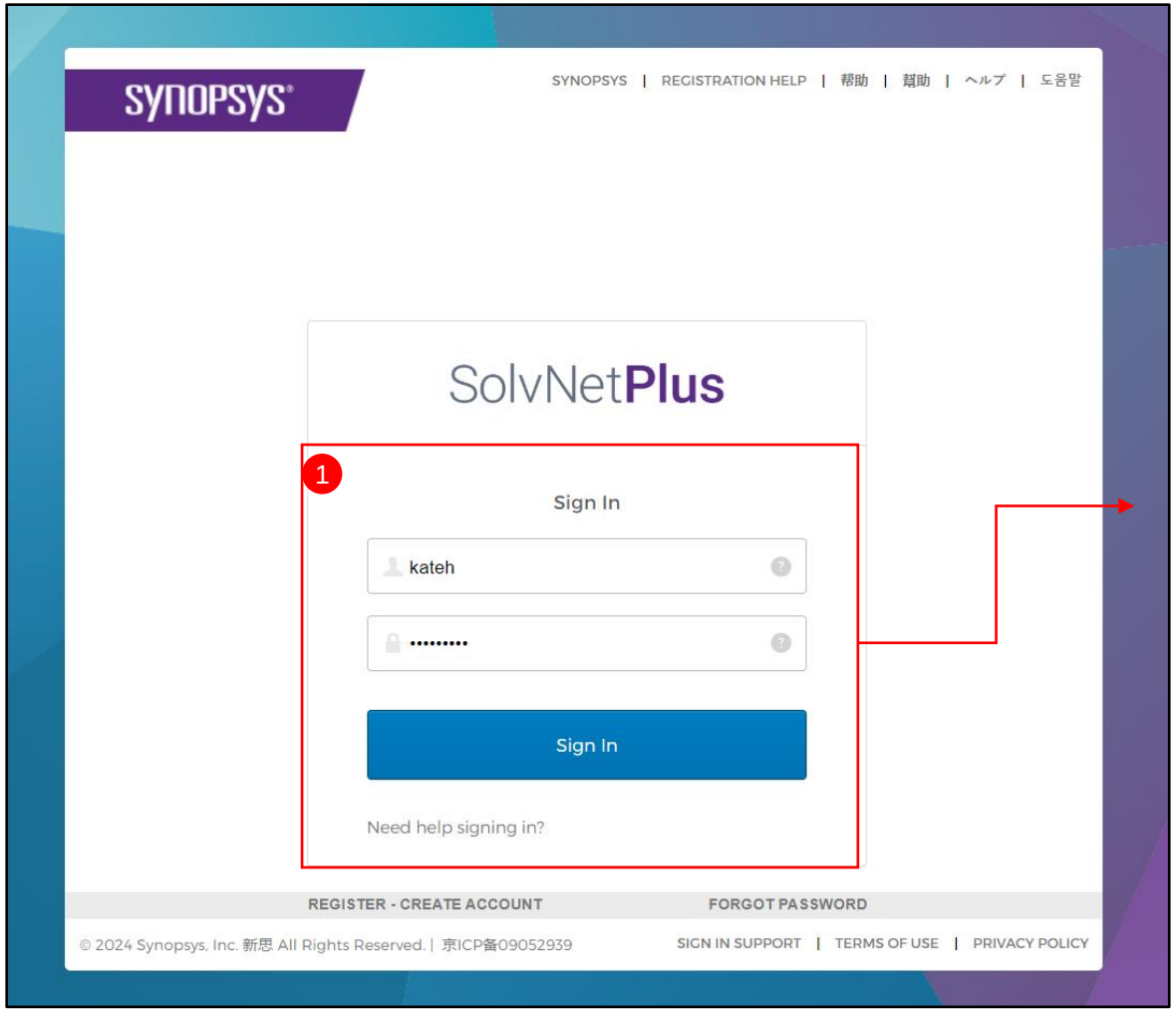
Search –
Provides an advanced search engine to retrieve information from various sources, such as documentation, articles, training, and so on.

Training –
Access Synopsys Learning Center for free self-paced training resources.

Document –
contains product release note, installation guide, user guide & reference manual



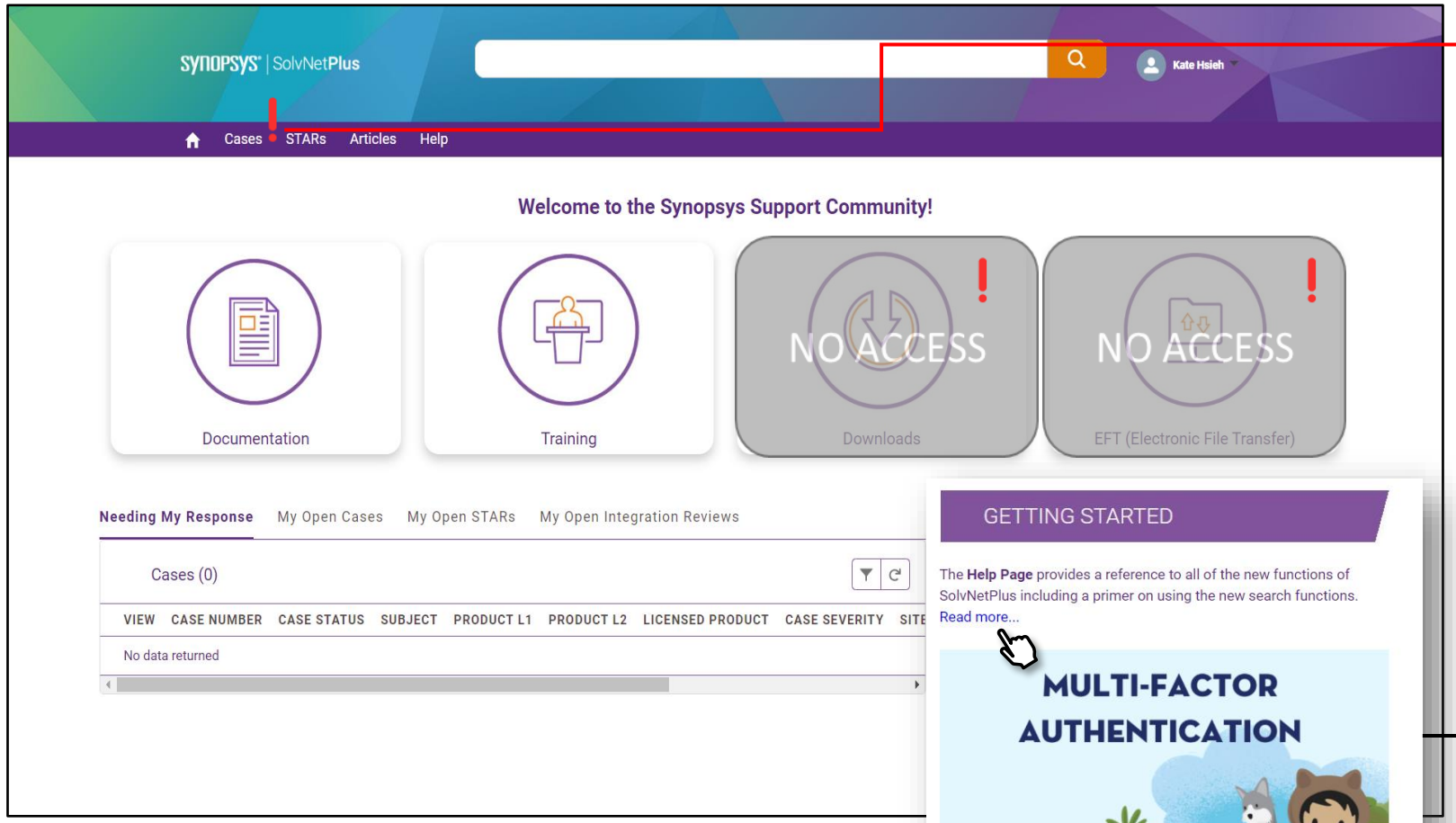
Log-in to SolvNetPlus



1 Log-in with Synopsys SolvNetPlus credential

Link:
https://solvnetplus.synopsys.com/s/

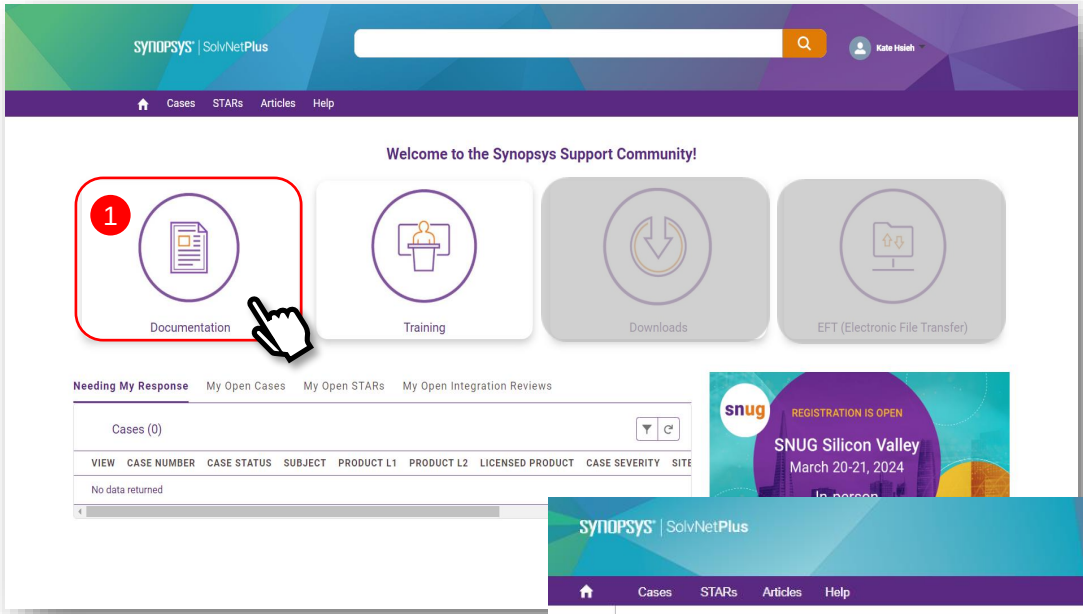
Get started



University users can access Documentation, Training & Search; but CANNOT access Download, EFT, Cases & STARs.

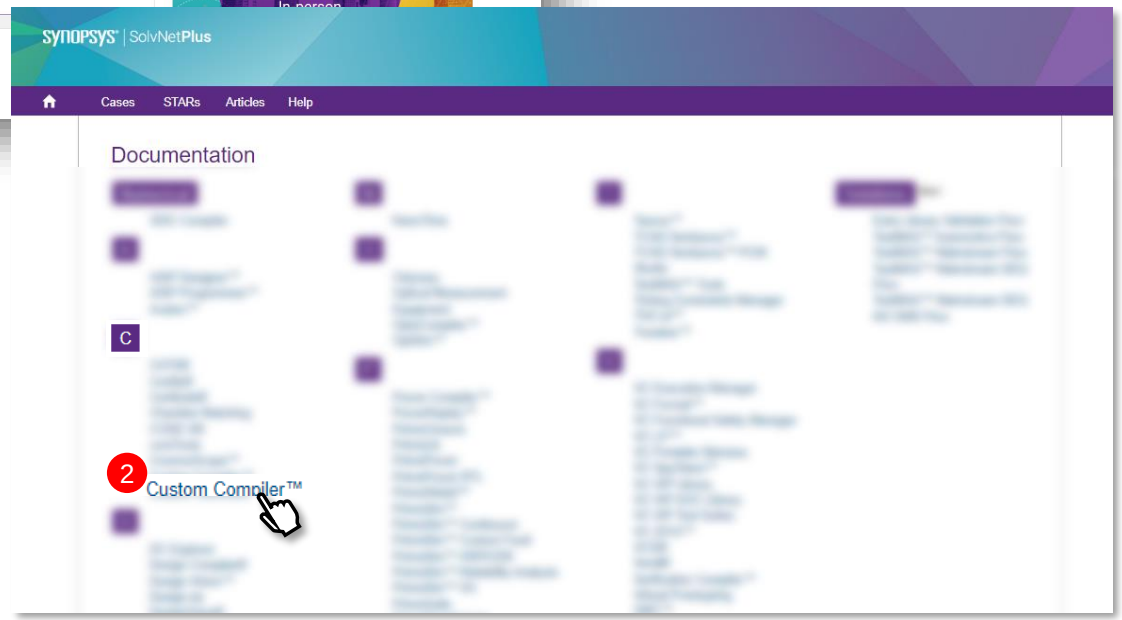
Read “ GETTING STARTED” before use

Documentation



1 Click on “Documentation”

2 Search by product name to get tool documents. You can download release notes, installation guides & user guides and reference manuals from this section

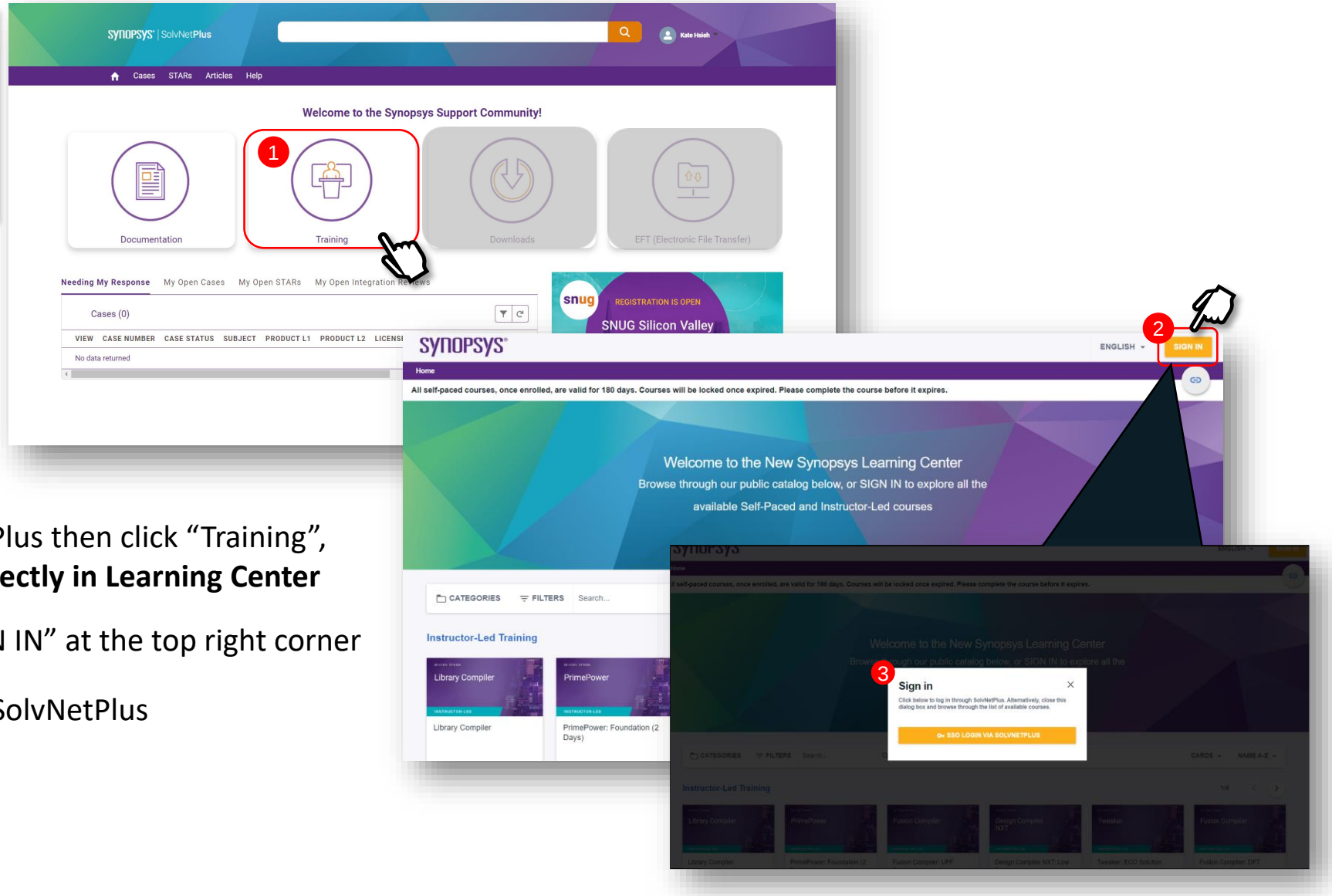


Training

Documentation

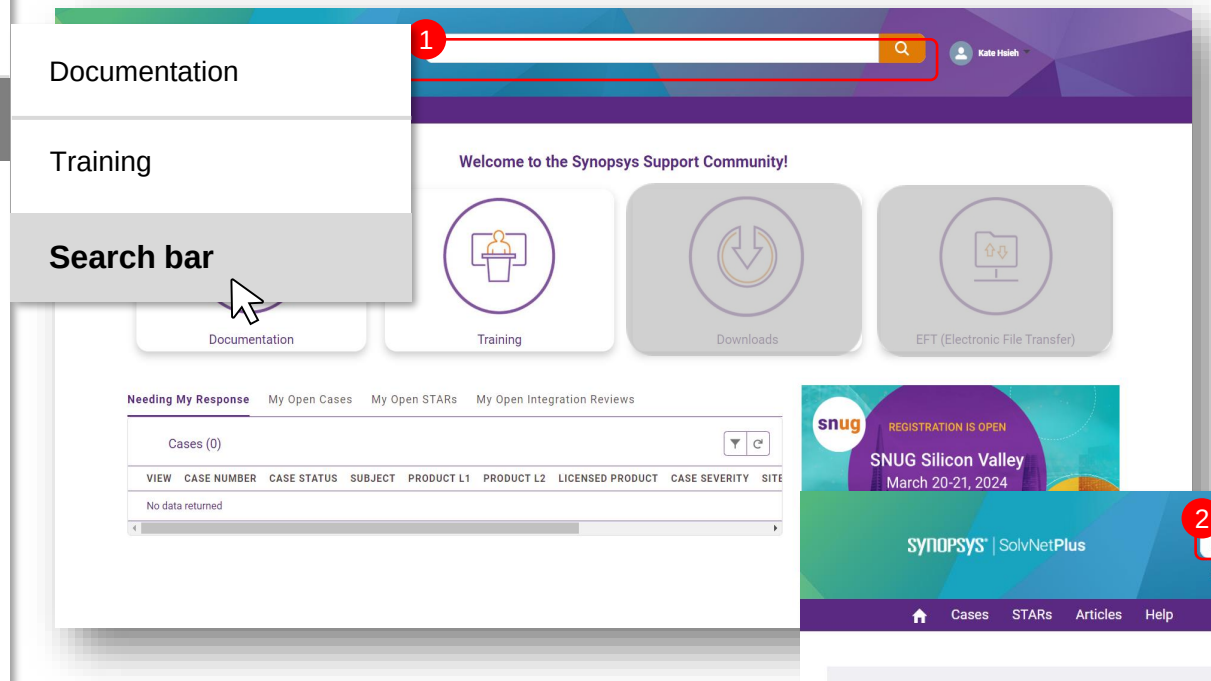
Training

Search bar



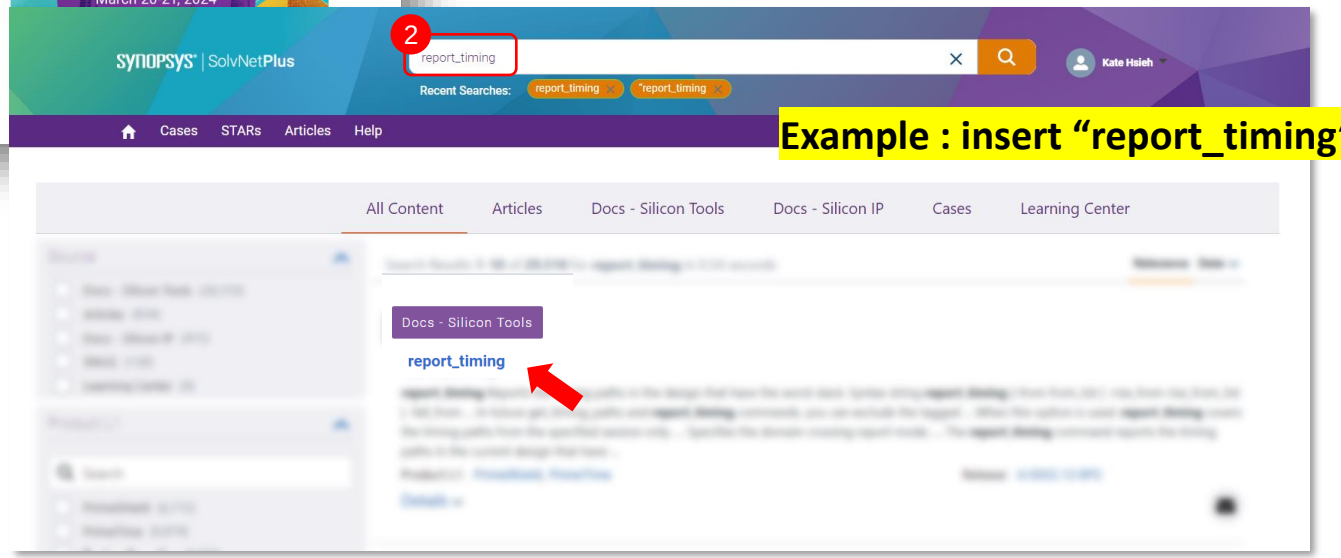
1. Login SolvNetPlus then click “Training”, **you will be directly in Learning Center**
2. Click the “SIGN IN” at the top right corner
3. SSO Login via SolvNetPlus

Search bar



1. Look for information in the “Search” bar. You can use search to retrieve information from various sources

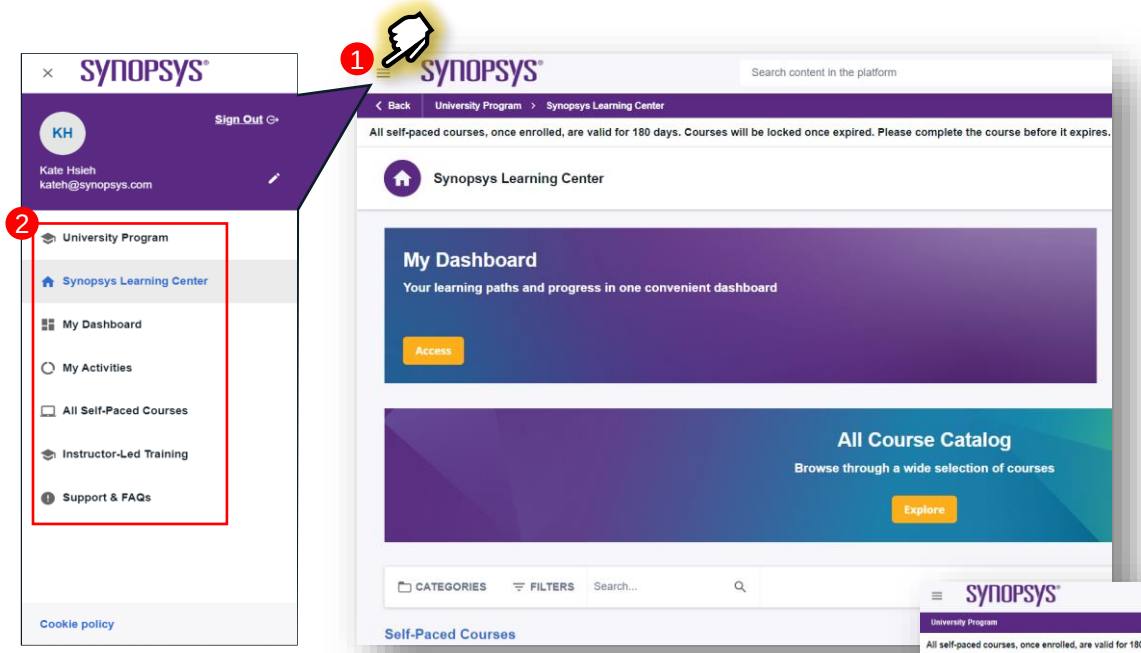
2. Choose needed info from the displayed search results. The information will be displayed from various sources, such as documentation, articles, training, YouTube, and so on **(but NOT in cases & STARs)**



Example : insert “report_timing”

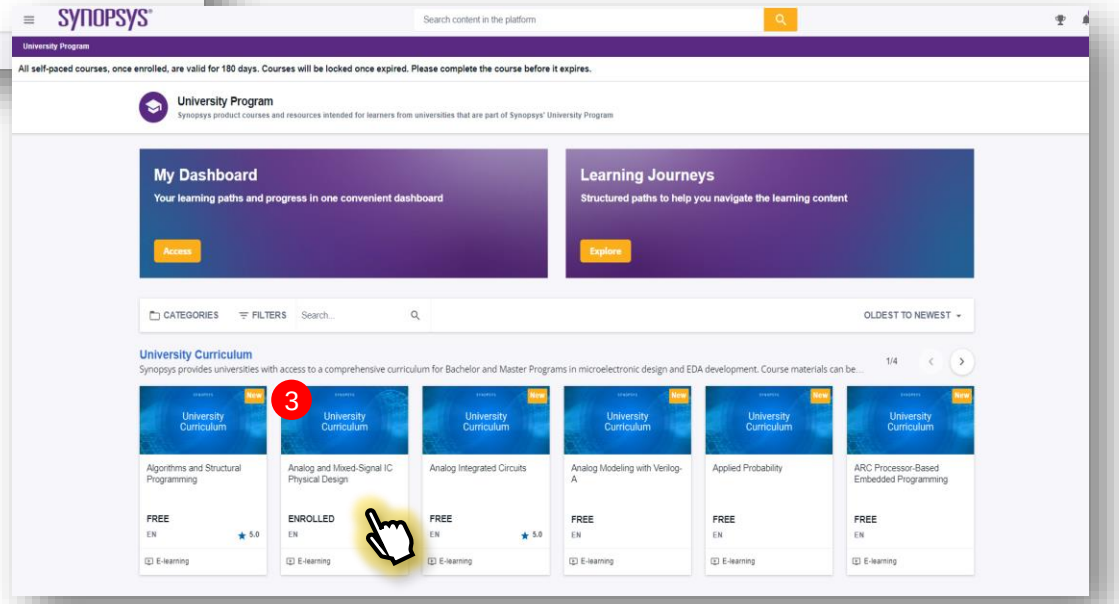
Synopsys Learning Center

Access Synopsys Learning Center



1. Click on "三"
2. Select the page which you want to visit based on the categories.
3. Choose the "University Curriculum"

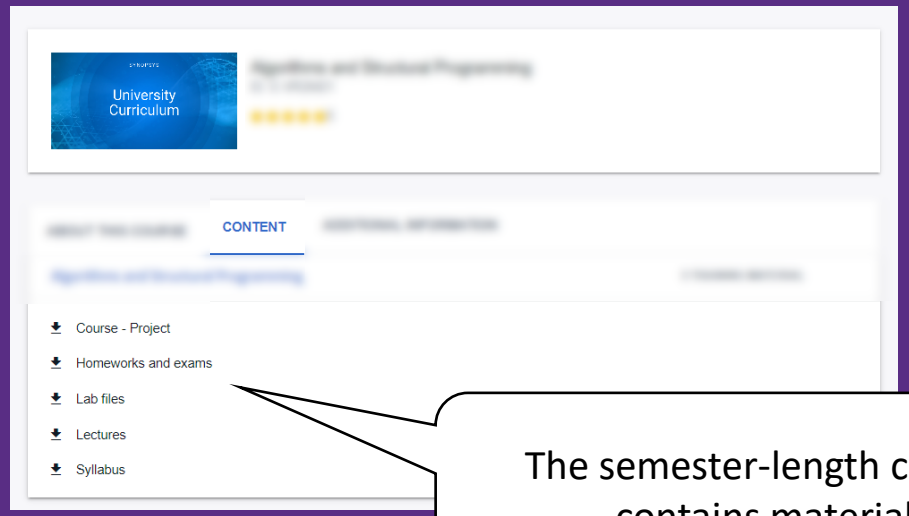
Link: [Synopsys Learning Center]



University Curriculum

Synopsys provides universities with access to a comprehensive curriculum for Bachelor and Master Programs in microelectronic design and EDA development. Course materials can be used to implement a new course or to supplement content in an existing course. Search courses by keyword or course type to find and download courses quickly and easily.

Types of Learning - E-learning

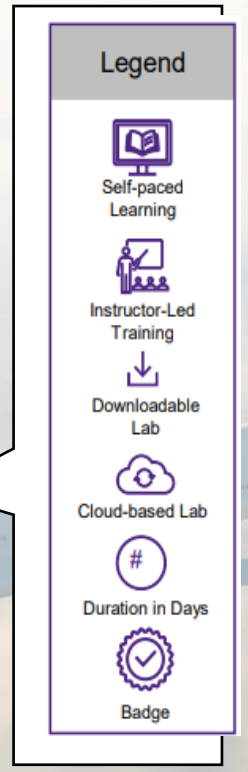


The semester-length course contains material

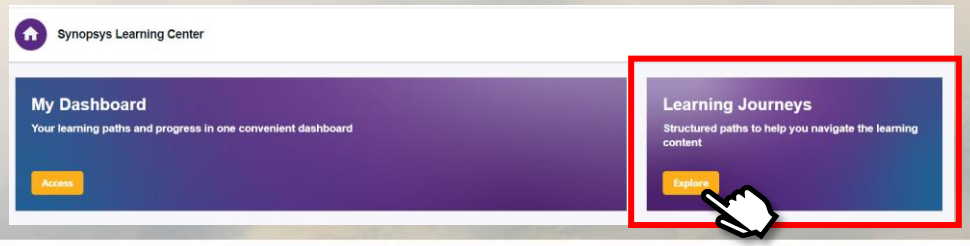
Synopsys Learning Paths

▼ Recommended for an Analog Designer

Course 1	Course 2	Course 3	Course 4	Course 5
CC: Foundation I	CC: Schematic Entry	PrimeWave Jumpstart	PrimeWave & PrimeSIM SPICE Analog Tutorial	CC: Reliability
Custom Compiler Overview	Capturing Schematics	Testbench Setup	OP, DC, Tran Analysis	PrimeSim ResCheck Analysis
Library Manager	Using Advanced Editing features	Parametric Analysis	Loop Stability Analysis	PrimeSim EMIR Reliability Analysis
Data I/0	Generating Symbols	Corner Analysis	Noise Analysis	In-Design EM Aware Layout Implementation
Technology	Schematic Entry	Monte Carlo Analysis	Transient Analysis	In-Design Capacitance Reporting
Design Review Assistant	Advanced Schematic Editing	Dynamic Device Checks	Transient Noise Analysis	In-Design Resistance Checking and Reporting
Unified Constraint Management	Symbol Creation		S-parameter Analysis	Partial Layout Extraction (needs CC Elite license)
	Design Hierarchy		SOA	Layout Dependent Effects
	Working with Text Views		Transient + Monte Carlo Analysis	Voltage Dependent Rule Check
	Parameterized Connections		MOSRA	
	Schematic Overlays			
	Using Estimated Parasitic			



Learning Paths are available on Synopsys Learning Center→
Learning Journeys



2 Curriculum

IC Design Curriculum/EDA Curriculum

IC Design Curriculum	
Bachelor Degree Courses	• Introduction to Semiconductor Devices • Introduction to Circuits • IC Design Introduction • Digital Integrated Circuits • Semiconductor Technology • Analog Integrated Circuits • Microprocessor Systems • IC Simulation Theory • Logic Design • IC Synthesis and Optimization • IC Physical Design • IC Testing
Master Degree Courses	• Mixed-Signal IC Design • FPGA Prototyping • I/O Design • Design for Test • Low Power Design • Design of Embedded Systems • Rad-hard IC Design • RF IC Design • Crosstalk and Noise • Modeling and Optimization of IC Interconnects • IC Reliability • IC Physical Design Algorithms

EDA Curriculum	
Bachelor Degree Courses	• EDA Introduction • Discrete Mathematics and Probability • EDA Mathematical Methods • Programming C++ • Hardware Description Languages • Theory of Algorithms • Object-Oriented Programming • Operating Systems and System Programming • Scripting Languages • Software Development Technology Computational Geometry • Data Structures • Unix System Administration • Technical Writing
Master Degree Courses	• Linear Algebra • Big Data • Contemporary Software Development Kits • EDA Tools • IC Physical Design Algorithms • Compilers Design • Digital Signal Processing • Numerical Methods • Probability Theory and Mathematical Statistics • Databases • Operational Research • IC Verification Algorithms

Advanced Courses/General Courses

Advanced Courses

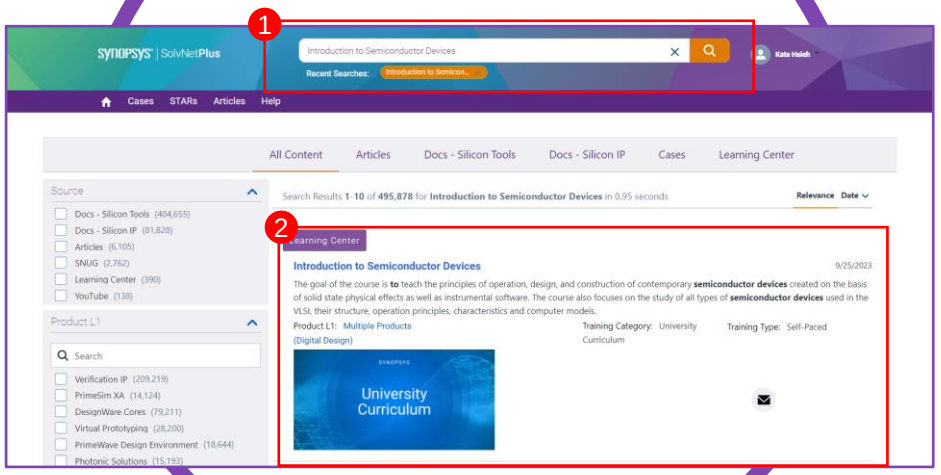
Bachelor Degree Courses	• Analog and Mixed-Signal IC Physical Design • Custom Analog Design Flow Tutorial • Statistical Techniques for Timing Analysis: Current State and Trends • Thermal and Electro-Thermal Simulation: Achievements and Trends • Signal and Power Integrity: Current State and New Approaches • Verification Methodologies for Low Power • Characterization with SiliconSmart • Signal Processing and Systems Theory
Master Degree Courses	• High Speed SerDes Design • Synopsys EDA Tool Flow for Back-End Digital IC Design • Synopsys EDA Tool Flow for Front-End Digital IC Design • IC Synthesis and Optimization with Fusion Compiler • Advanced Methods in Logic Synthesis and Equivalence Checking • Low Power Design with SAED 14nm EDK • Low Power Methodology Manual for 14nm • Memory PHY and DRAM • Soft IP Development • Universal Verification Methodology • Analog Modeling with Verilog-A

General Courses

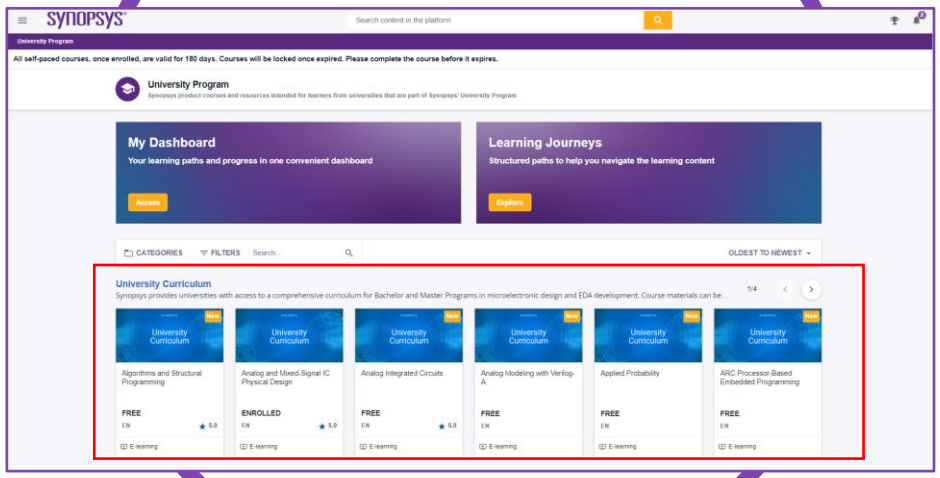
Bachelor Degree Courses	• Numerical and Logic Bases of Digital Circuits • Electrotechnical Bases of Electronic Circuits • Chip Design • Static Timing Analysis • IC Fabrication • Fundamentals of Telecommunications • Introduction to RF Communication • RF Circuits • Applied Probability • Python • Tool Command Language (TCL) • Scripting Languages for Beginners • Programming Languages and Compilers Verilog • Computer Networks • Fuzzy Logic • LINUX System and Network Administration	• Computer Architecture and Engineering • Algorithms and Structural Programming • Database Management System • IC Schematic Design Algorithms • Introduction to Algorithms • User Interface Design • ARC Processor-Based Embedded Programming • How to Create an Interoperable PDK • Physical Verification Runset Development
Master Degree Courses	• IC Design Flow • Synopsys Design Flow Tutorial • IC Design for Thermal Issues • SystemVerilog • Operational Calculus • Optimization Methods • Complex Functions • Fourier Transformations • Computer Language Engineering • Design of Programming Languages • IC Design Algorithms • Compiler Optimization and Code Generation	

How to find the Courses?

1 From SolvNetPlus



2 From Learning Center



1. Type the name of the course you want to search for in the search bar
2. Get the search results

Directly access [Synopsys Learning Center] to find the courses.

Libraries, PDKS, and Memory Compiler

Generic Libraries (EDK)

- 14nm, 32/28nm and 90nm
- Enables students to master advanced design methods using the latest Synopsys EDA tools
- Includes:

Digital Standard Cell Library	I/O Cell Library	I/O Special Cell Library	Embedded Memories
Phase Locked Loop	Low Power Memories	Reference Designs	

- Used by Synopsys for:

Curricula Development	Customer Education	Global Technical Services	Application Consultants
To support development of laboratory works and course projects.	To train customers with Leon3 and ORCA processors' design.	To train internal staff and customers on Synopsys tools and low power flows.	To develop and test sample designs and Reference Methodology scripts.

Interoperable Process Design Kits (iPDKs)

- 32/28nm and 90nm
- Enables students to master AMS/Custom design with the Synopsys custom implementation tool suite
- Includes:

Technology Files	Parasitic Extraction Files	Symbol Library and Python PCells	Embedded Memories
Physical Verification Files	HSPICE Models	Callback Scripts	Setup Files

- Used by Synopsys for:

Curricula Development	Customer Education	Global Technical Services	Application Consultants
To support development of laboratory works and course projects.	To train customers with Leon3 and ORCA processors' design.	To train internal staff and customers on Synopsys tools and low power flows.	To develop and test sample designs and Reference Methodology scripts.

Synopsys Generic Memory Compiler

- Configurable software that automatically generates static RAM circuits of different types and sizes with all required deliverables
- Generate custom memory instances for educational ICs
- Designed for use with Synopsys EDKs and EDA tools
- Optimized for the Synopsys Digital Design Flow
- Supports multiple technologies (90nm, 32/28nm, etc.)

User interface

- Command line
- GUI

Supported memory types

- 1 port SRAM
- 2 port SRAM
- 1 port Low Power SRAM
- 2 port Low Power SRAM

*"Using the Synopsys Generic Memory Compiler in our complex processor for DSP application was a **great time-saving tool**. It helped the students generate the SRAM they wanted in a snap, saving them critical time to concentrate on the rest of the complex design."*

Dr. Maged Ghoneima, American University in Cairo

Thank You

Synopsys Academic & Research Alliances (SARA) Taiwan

Contact us tw-up@synopsys.com Global Home Page TW Home Page