



# A Quick Guide to University Software Program

Courseware, SolvNetPlus & Synopsys Learning Center

February 2024

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# About SARA

# What is Synopsys Academic & Research Alliances (SARA) ?



Through innovative collaborations, shared programs, and access to advanced technologies, Synopsys Academic & Research Alliances (SARA) is dedicated to furthering university research and education in the field of electronic design.

By investing in science, technology, engineering, and mathematics (STEM) education, we aim to nurture the interests and skills that are needed to bring the next generation of engineers into the workforce and the research labs.



# Who we help



## Student

Empower and educate the next generation of engineers to be ready to tackle the latest challenges, whether in research or in industry.



## Educator

Provide learning opportunities and training materials while lowering the barriers to access Synopsys technology for education and research.



## Researchers

Address the ever-evolving challenges of the semiconductor industry, uncover new solutions, and pave the path toward future technologies.



## Entrepreneurs

Collaborate to discover new technologies and turn fresh ideas into market-ready products for our Smart Everything world.

# University Software Program Membership Benefits



## SolvNetPlus

A repository of self-help resources to resolve many support issues, provide access to training, and many educational materials.



## Synopsys Learning Center

Synopsys Learning Center offers a wide range of courses (**short training, instructor led, quick tips**) in different delivery modes and allows easier navigation and a more personalized learning experience, all while using your SolvNetPlus credentials.



## Curriculum

Semester-length course contains material including **syllabus, lectures, labs, homework, and exams**. Synopsys tools are applied in the labs for a thorough and practical understanding of theoretical concepts introduced in each course.



## Libraries, PDKs, and Memory Compiler

Teaching resources are offered to ensure students gain valuable experience using a complete design flow and to master advanced design methods such as low power and analog/mixed signal.



## Reference Methodology Retrieval System

RMgen provides an easy way to configure and download product-specific and release-specific reference methodology scripts. These scripts are a starting point for developing product-specific flow scripts. Customize the scripts to work in your design environment.

# SolvNetPlus

# What is SolvNetPlus?

[SolvNetPlus](#) provides **Documentation, Training, and a comprehensive, searchable knowledge base** that provides solutions to frequently encountered problems.

## Training –

Access Synopsys Learning Center for free self-paced training resources.

## Search –

Provides an advanced search engine to retrieve information from various sources, such as documentation, articles, training, and so on.

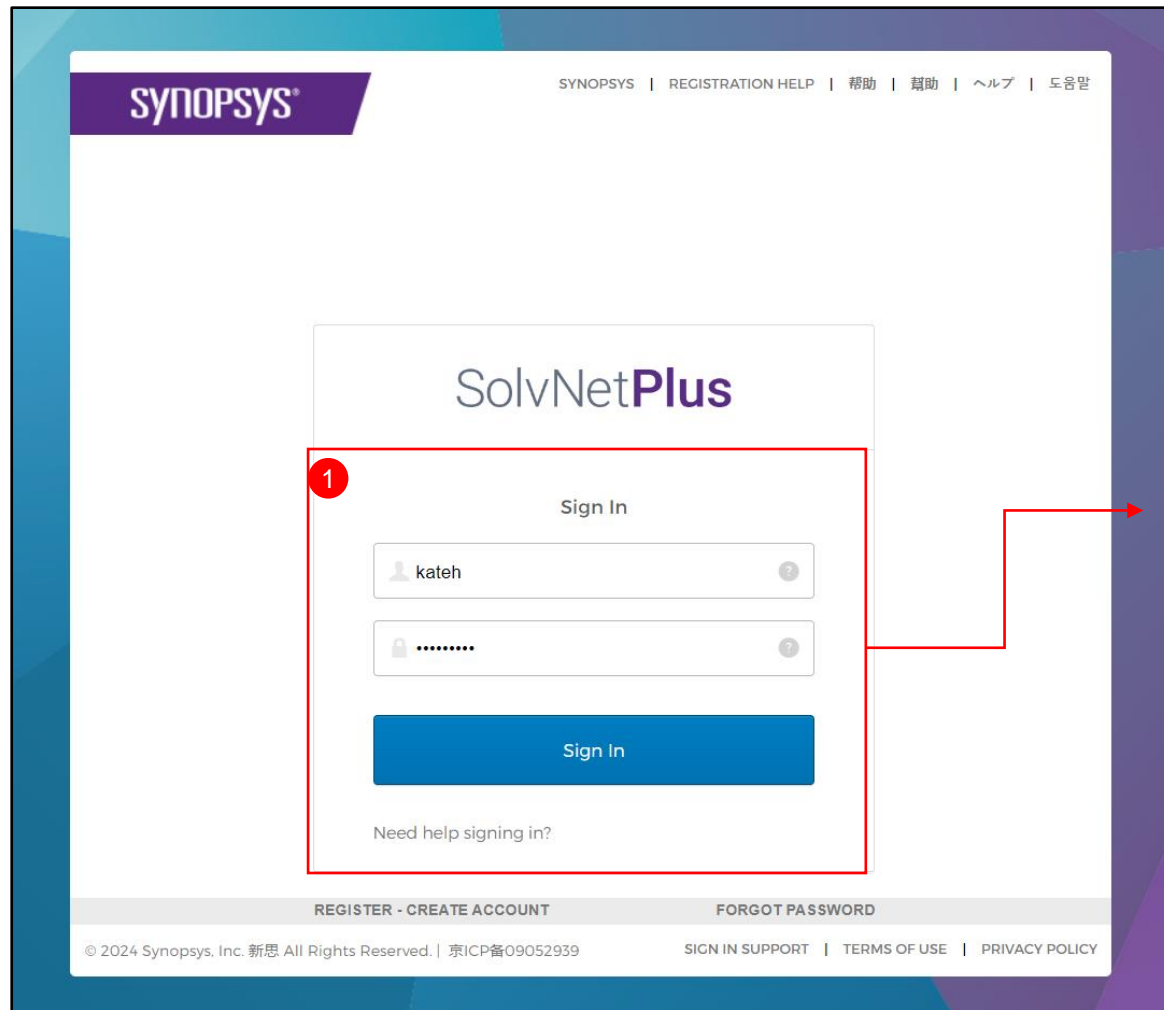
## Document –

contains product release note, installation guide, user guide & reference manual

The screenshot shows the Synopsys SolvNetPlus website. The header includes the Synopsys logo and 'SolvNetPlus' text. A navigation bar contains links for 'Cases', 'STARs', 'Articles', and 'Help'. A search bar and a user profile for 'Kate Hsieh' are visible. The main content area features a welcome message and four large buttons: 'Documentation' (with a document icon), 'Training' (with a person at a podium icon), 'Downloads' (with a circular arrow icon and 'NO ACCESS' text), and 'EFT (Electronic File Transfer)' (with a folder icon and 'NO ACCESS' text). Three callout boxes provide additional information: one for 'Document' (pointing to the Documentation button), one for 'Training' (pointing to the Training button), and one for 'Search' (pointing to the search bar).



# Log-in to SolvNetPlus



1 Log-in with Synopsys SolvNetPlus credential

Link:

<https://solvnetplus.synopsys.com/s/>

# Get started

Log-in to SolvNetPlus

Get started

Key features

SYNOPSYS | SolvNetPlus

Search

Kate Hsieh

Home Cases STARs Articles Help

Welcome to the Synopsys Support Community!

Documentation Training Downloads EFT (Electronic File Transfer)

NO ACCESS NO ACCESS

Needing My Response My Open Cases My Open STARs My Open Integration Reviews

| VIEW             | CASE NUMBER | CASE STATUS | SUBJECT | PRODUCT L1 | PRODUCT L2 | LICENSED PRODUCT | CASE SEVERITY | SITE |
|------------------|-------------|-------------|---------|------------|------------|------------------|---------------|------|
| No data returned |             |             |         |            |            |                  |               |      |

GETTING STARTED

The **Help Page** provides a reference to all of the new functions of SolvNetPlus including a primer on using the new search functions. [Read more...](#)

**MULTI-FACTOR AUTHENTICATION**

SolvNetPlus is now enforcing MFA (Multi-Factor Authentication) during the login process. A one-time passcode will be sent via email and will be required to access SolvNetPlus. [Read more...](#)

! University users can access Documentation, Training & Search; but CANNOT access Download, EFT, Cases & STARs.

Read "GETTING STARTED" before use

# Documentation

Log-in to SolvNetPlus

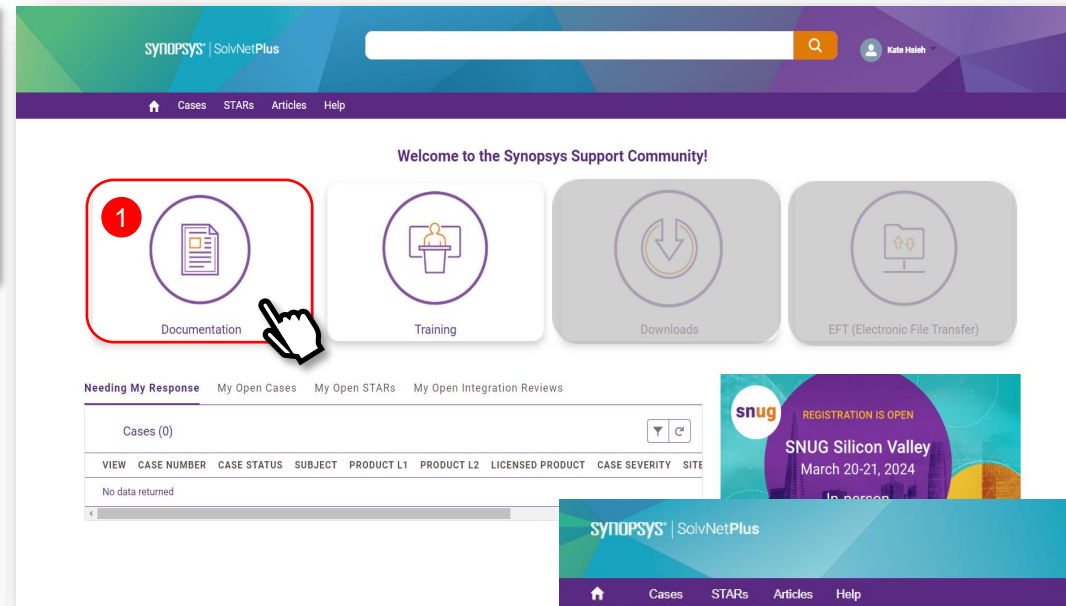
Get started

Key features >

Documentation

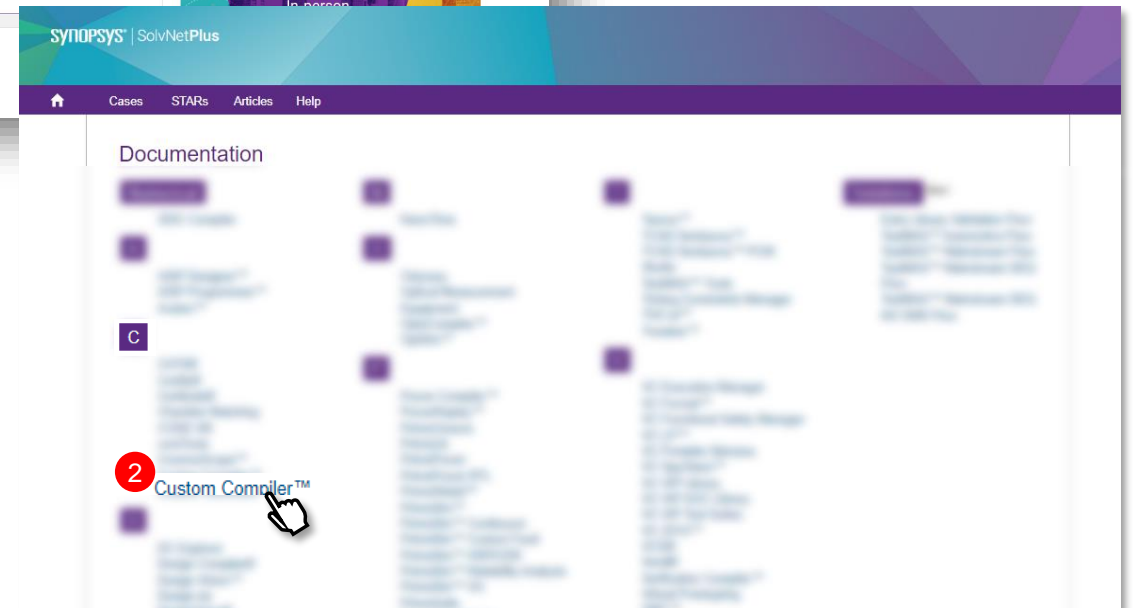
Training

Search bar



1 Click on “Documentation”

- 2 Search by product name to get tool documents. You can download release notes, installation guides & user guides and reference manuals from this section



# Training

Get started w/ SolvNetPlus

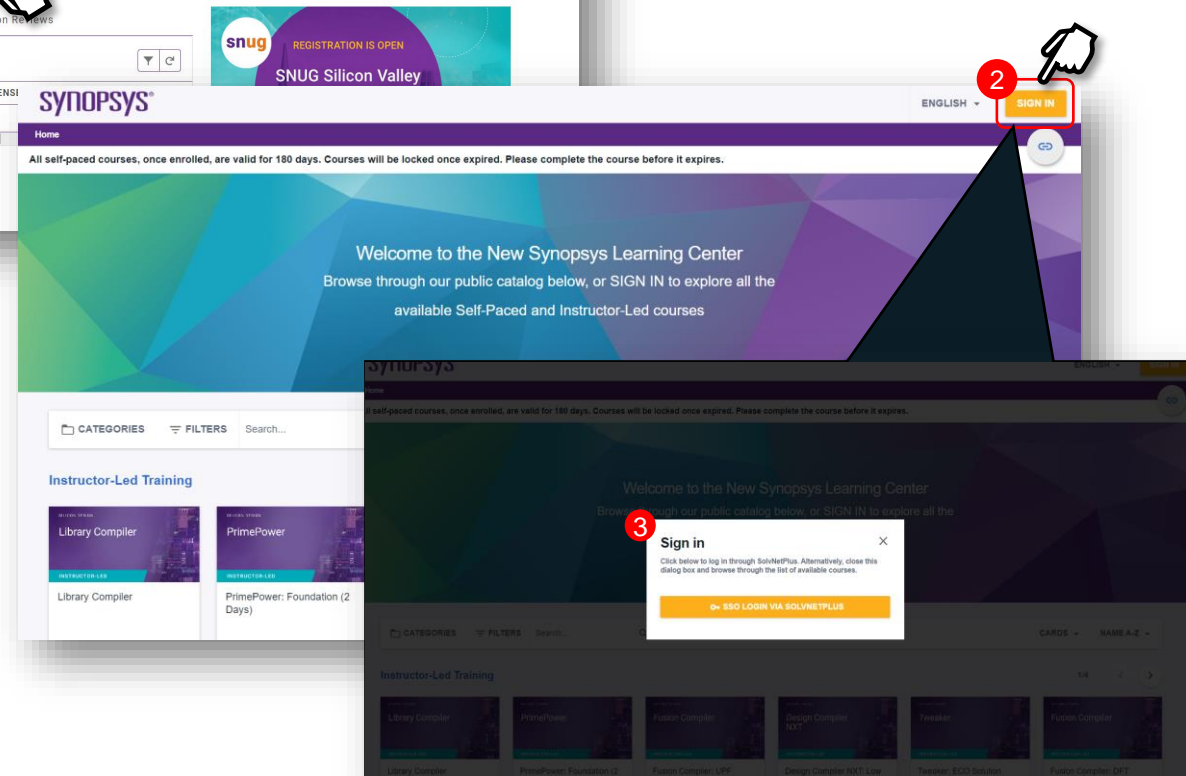
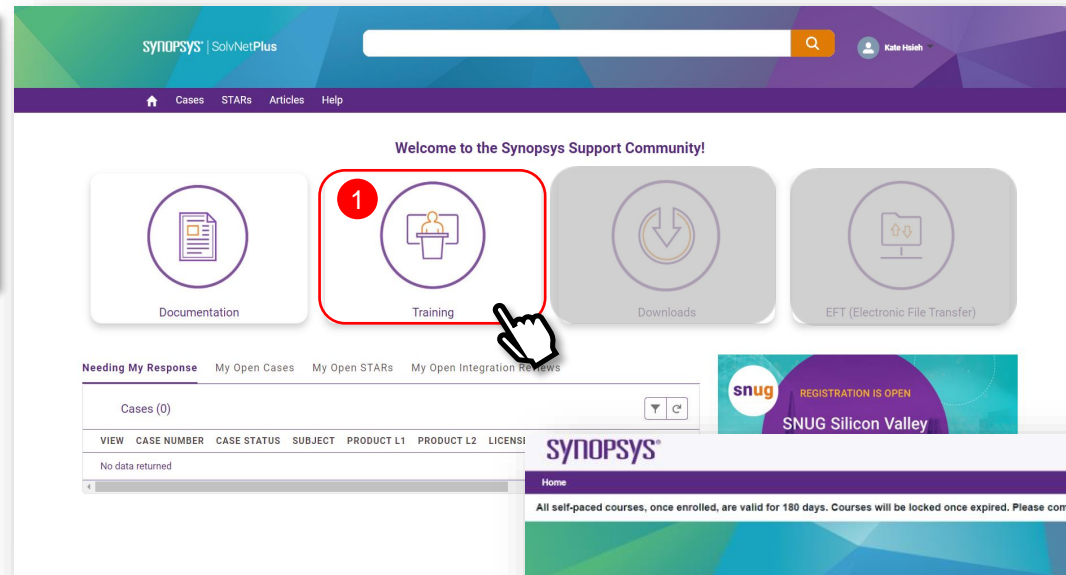
Notice

Key features >

Documentation

**Training**

Search bar



- 1 Login SolvNetPlus then click “Training”, you will be directly in Learning Center
- 2 Click the “SIGN IN” at the top right corner
- 3 SSO Login via SolvNetPlus

# Search bar

Get started w/ SolvNetPlus

Notice

Key features &gt;

Documentation

Training

Search bar

Welcome to the Synopsys Support Community!

Documentation Training Downloads EFT (Electronic File Transfer)

Needing My Response My Open Cases My Open STARs My Open Integration Reviews

Cases (0)

| VIEW             | CASE NUMBER | CASE STATUS | SUBJECT | PRODUCT L1 | PRODUCT L2 | LICENSED PRODUCT | CASE SEVERITY | SITE |
|------------------|-------------|-------------|---------|------------|------------|------------------|---------------|------|
| No data returned |             |             |         |            |            |                  |               |      |

REGISTRATION IS OPEN  
SNUG Silicon Valley  
March 20-21, 2024

SYNOPSYS | SolvNetPlus

report\_timing

Recent Searches: report\_timing report\_timing

Home Cases STARs Articles Help

- 1 Look for information in the “Search” bar. You can use search to retrieve information from various sources
- 2 Choose needed info from the displayed search results. The information will be displayed from various sources, such as documentation, articles, training, YouTube, and so on (**but NOT in cases & STARs**)

Example : insert “report\_timing”

All Content Articles Docs - Silicon Tools Docs - Silicon IP Cases Learning Center

report\_timing

Docs - Silicon Tools

report\_timing

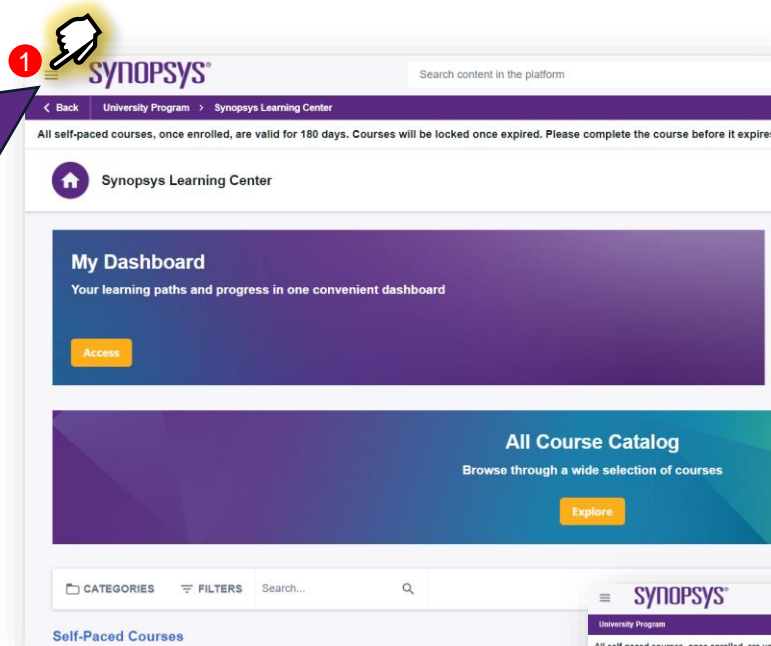
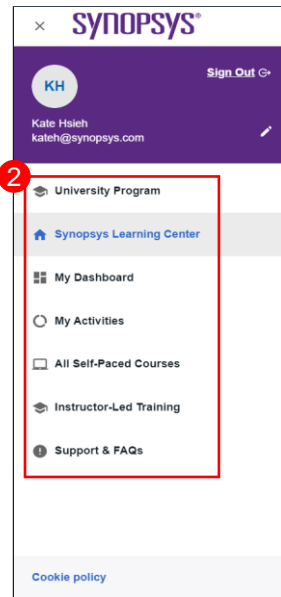
# Synopsys Learning Center

# Access Synopsys Learning Center

Access Synopsys Learning Center

University Curriculum

Synopsys Learning Paths

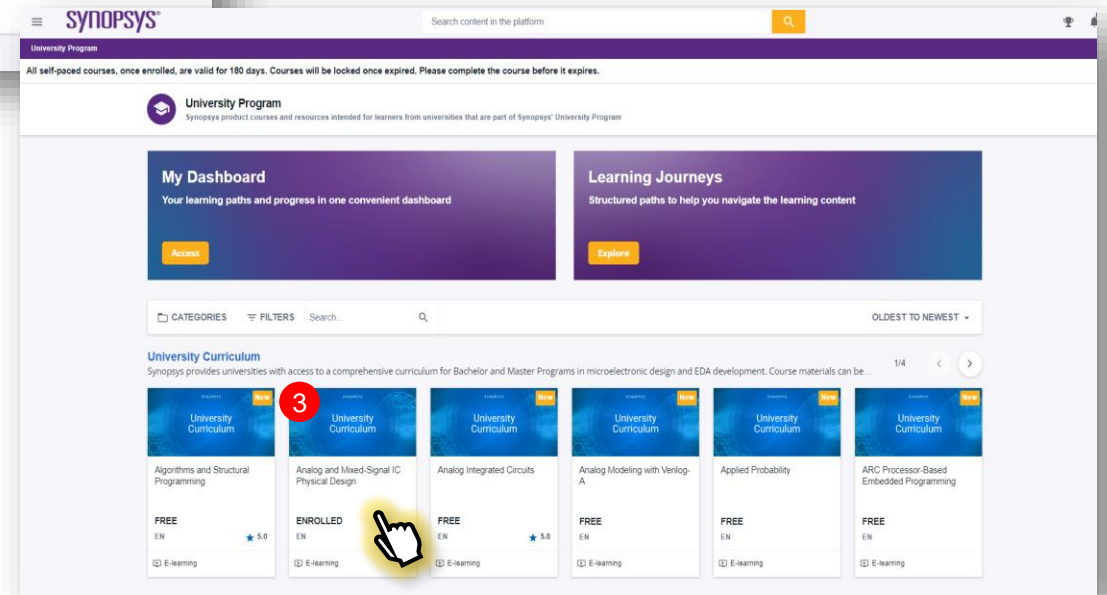


1 Click on “☰”

2 Select the page which you want to visit based on the categories.

3 Choose the “University Curriculum”

Link: [Synopsys Learning Center](#)



Access Synopsys Learning Center

University Curriculum

Synopsys Learning Paths

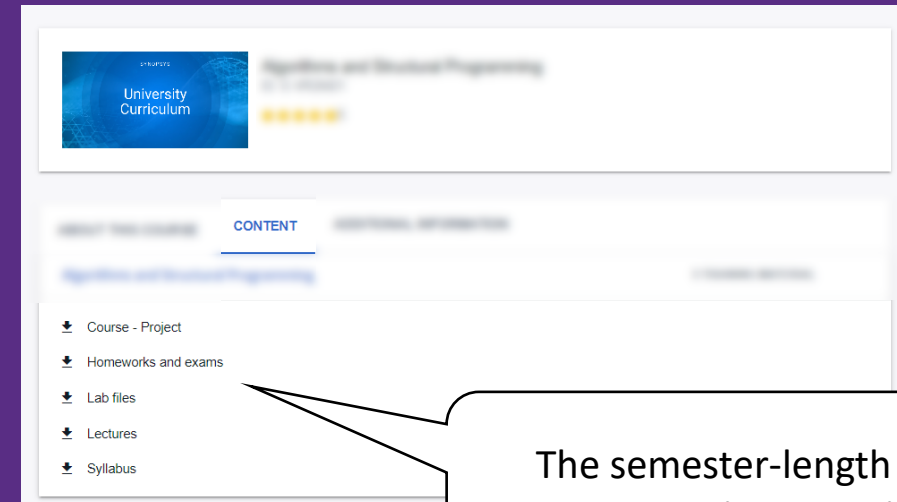


# University Curriculum

Synopsys provides universities with access to a comprehensive curriculum for Bachelor and Master Programs in microelectronic design and EDA development. Course materials can be used to implement a new course or to supplement content in an existing course. Search courses by keyword or course type to find and download courses quickly and easily.



## Types of Learning - E-learning



The semester-length course contains material



## Synopsys Learning Paths

▼ Recommended for an Analog Designer

Access Synopsys Learning Center

Types of Learning

Synopsys Learning Paths

| Course 1 →                    | Course 2 →                      | Course 3 →                 | Course 4 →  | Course 5   |
|-------------------------------|---------------------------------|----------------------------|---|--|
| <b>CC: Foundation I</b>       | <b>CC: Schematic Entry</b>      | <b>PrimeWave Jumpstart</b> | <b>PrimeWave &amp; PrimeSIM SPICE Analog Tutorial</b> | <b>CC: Reliability</b>                             |
| Custom Compiler Overview      | Capturing Schematics            | Testbench Setup            | OP, DC, Tran Analysis                                 | PrimeSim ResCheck Analysis                         |
| Library Manager               | Using Advanced Editing features | Parametric Analysis        | Loop Stability Analysis                               | PrimeSim EMIR Reliability Analysis                 |
| Data I/O                      | Generating Symbols              | Corner Analysis            | Noise Analysis  | In-Design EM Aware Layout Implementation           |
| Technology                    | Schematic Entry                 | Monte Carlo Analysis       | Transient Analysis                                    | In-Design Capacitance Reporting                    |
| Design Review Assistant       | Advanced Schematic Editing      | Dynamic Device Checks      | Transient Noise Analysis                              | In-Design Resistance Checking and Reporting        |
| Unified Constraint Management | Symbol Creation                 |                            | S-parameter Analysis                                  | Partial Layout Extraction (needs CC Elite license) |
|                               | Design Hierarchy                |                            | SOA   | Layout Dependent Effects                           |
|                               | Working with Text Views         |                            | Transient + Monte Carlo Analysis                      | Voltage Dependent Rule Check                       |
|                               | Parameterized Connections       |                            | MOSRA   |  |
|                               | Schematic Overlays              |                            |   |  |
|                               | Using Estimated Parasitic       |                            |   |  |
|                               |                                 |                            |   |  |

### Legend

- Self-paced Learning
- Instructor-Led Training
- Downloadable Lab
- Cloud-based Lab
- Duration in Days
- Badge

Learning Paths are available on Synopsys Learning Center →  
**Learning Journeys**

Synopsys Learning Center

**My Dashboard**  
Your learning paths and progress in one convenient dashboard

[Access](#)

**Learning Journeys**  
Structured paths to help you navigate the learning content

[Explore](#)

## 2 Curriculum

# IC Design Curriculum/EDA Curriculum

| IC Design Curriculum           |   |
|--------------------------------|---|
| <b>Bachelor Degree Courses</b> | <ul style="list-style-type: none"> <li>• Introduction to Semiconductor Devices</li> <li>• Introduction to Circuits</li> <li>• IC Design Introduction</li> <li>• Digital Integrated Circuits</li> <li>• Semiconductor Technology</li> <li>• Analog Integrated Circuits</li> <li>• Microprocessor Systems</li> <li>• IC Simulation Theory</li> <li>• Logic Design</li> <li>• IC Synthesis and Optimization</li> <li>• IC Physical Design</li> <li>• IC Testing</li> </ul> |
| <b>Master Degree Courses</b>   | <ul style="list-style-type: none"> <li>• Mixed-Signal IC Design</li> <li>• FPGA Prototyping</li> <li>• I/O Design</li> <li>• Design for Test</li> <li>• Low Power Design</li> <li>• Design of Embedded Systems</li> <li>• Rad-hard IC Design</li> <li>• RF IC Design</li> <li>• Crosstalk and Noise</li> <li>• Modeling and Optimization of IC Interconnects</li> <li>• IC Reliability</li> <li>• IC Physical Design Algorithms</li> </ul>                              |

| EDA Curriculum                 |   |
|--------------------------------|---|
| <b>Bachelor Degree Courses</b> | <ul style="list-style-type: none"> <li>• EDA Introduction</li> <li>• Discrete Mathematics and Probability</li> <li>• EDA Mathematical Methods</li> <li>• Programming C++</li> <li>• Hardware Description Languages</li> <li>• Theory of Algorithms</li> <li>• Object-Oriented Programming</li> <li>• Operating Systems and System Programming</li> <li>• Scripting Languages</li> <li>• Software Development Technology Computational Geometry</li> <li>• Data Structures</li> <li>• Unix System Administration</li> <li>• Technical Writing</li> </ul> |
| <b>Master Degree Courses</b>   | <ul style="list-style-type: none"> <li>• Linear Algebra</li> <li>• Big Data</li> <li>• Contemporary Software Development Kits</li> <li>• EDA Tools</li> <li>• IC Physical Design Algorithms</li> <li>• Compilers Design</li> <li>• Digital Signal Processing</li> <li>• Numerical Methods</li> <li>• Probability Theory and Mathematical Statistics</li> <li>• Databases</li> <li>• Operational Research</li> <li>• IC Verification Algorithms</li> </ul>   |

# Advanced Courses/General Courses

| Advanced Courses               |   | General Courses                |   |   |
|--------------------------------|---|--------------------------------|---|---|
| <b>Bachelor Degree Courses</b> | <ul style="list-style-type: none"> <li>Analog and Mixed-Signal IC Physical Design</li> <li>Custom Analog Design Flow Tutorial</li> <li>Statistical Techniques for Timing Analysis: Current State and Trends</li> <li>Thermal and Electro-Thermal Simulation: Achievements and Trends</li> <li>Signal and Power Integrity: Current State and New Approaches</li> <li>Verification Methodologies for Low Power</li> <li>Characterization with SiliconSmart</li> <li>Signal Processing and Systems Theory</li> </ul>   | <b>Bachelor Degree Courses</b> | <ul style="list-style-type: none"> <li>Numerical and Logic Bases of Digital Circuits</li> <li>Electrotechnical Bases of Electronic Circuits</li> <li>Chip Design</li> <li>Static Timing Analysis</li> <li>IC Fabrication</li> <li>Fundamentals of Telecommunications</li> <li>Introduction to RF Communication</li> <li>RF Circuits</li> <li>Applied Probability</li> <li>Python</li> <li>Tool Command Language (TCL)</li> <li>Scripting Languages for Beginners</li> <li>Programming Languages and Compilers Verilog</li> <li>Computer Networks</li> <li>Fuzzy Logic</li> <li>LINUX System and Network Administration</li> </ul> | <ul style="list-style-type: none"> <li>Computer Architecture and Engineering</li> <li>Algorithms and Structural Programming</li> <li>Database Management System</li> <li>IC Schematic Design Algorithms</li> <li>Introduction to Algorithms</li> <li>User Interface Design</li> <li>ARC Processor-Based Embedded Programming</li> <li>How to Create an Interoperable PDK</li> <li>Physical Verification Runset Development</li> </ul> |
| <b>Master Degree Courses</b>   | <ul style="list-style-type: none"> <li>High Speed SerDes Design</li> <li>Synopsys EDA Tool Flow for Back-End Digital IC Design</li> <li>Synopsys EDA Tool Flow for Front-End Digital IC Design</li> <li>IC Synthesis and Optimization with Fusion Compiler</li> <li>Advanced Methods in Logic Synthesis and Equivalence Checking</li> <li>Low Power Design with SAED 14nm EDK</li> <li>Low Power Methodology Manual for 14nm</li> <li>Memory PHY and DRAM</li> <li>Soft IP Development</li> <li>Universal Verification Methodology</li> <li>Analog Modeling with Verilog-A</li> </ul> | <b>Master Degree Courses</b>   | <ul style="list-style-type: none"> <li>IC Design Flow</li> <li>Synopsys Design Flow Tutorial</li> <li>IC Design for Thermal Issues</li> <li>SystemVerilog</li> <li>Operational Calculus</li> <li>Optimization Methods</li> <li>Complex Functions</li> <li>Fourier Transformations</li> <li>Computer Language Engineering</li> <li>Design of Programming Languages</li> <li>IC Design Algorithms</li> <li>Compiler Optimization and Code Generation</li> </ul>   |   |

# How to find the Courses?

# 1

## From SolvNetPlus

The screenshot shows the Synopsys SolvNetPlus search results page. A search bar at the top contains the text "Introduction to Semiconductor Devices". Below the search bar, a sidebar on the left lists various content sources like "Docs - Silicon Tools", "Articles", "Docs - Silicon IP", "Cases", and "Learning Center". The main content area displays search results for "Introduction to Semiconductor Devices", including a course card with a "University Curriculum" thumbnail.

# 2

## From Learning Center

The screenshot shows the Synopsys University Program Learning Center dashboard. The dashboard features sections for "My Dashboard" and "Learning Journeys". Below these, there is a "University Curriculum" section displaying a grid of course cards, including "Algorithms and Structural Programming", "Analog and Mixed-Signal IC Physical Design", "Analog Integrated Circuits", "Analog Modeling with Verilog-A", "Applied Probability", and "ARC Processor-Based Embedded Programming".

- 1 Type the name of the course you want to search for in the search bar
- 2 Get the search results

Directly access [Synopsys Learning Center](#) to find the courses.

# Libraries, PDKS, and Memory Compiler

## Generic Libraries (EDK)

Interoperable Process Design Kits (iPDKs)

Synopsys Generic Memory Compiler

# Generic Libraries (EDK)

- 14nm, 32/28nm and 90nm
- Enables students to master advanced design methods using the latest Synopsys EDA tools
- Includes:

Digital Standard Cell Library

I/O Cell Library

I/O Special Cell Library

Embedded Memories

Phase Locked Loop

Low Power Memories

Reference Designs

- Used by Synopsys for:

Curricula Development

To support development of laboratory works and course projects.

Customer Education

To train customers with Leon3 and ORCA processors' design.

Global Technical Services

To train internal staff and customers on Synopsys tools and low power flows.

Application Consultants

To develop and test sample designs and Reference Methodology scripts.

Generic Libraries (EDK)

Interoperable Process Design Kits (iPDKs)

Synopsys Generic Memory Compiler

## Interoperable Process Design Kits (iPDKs)

- 32/28nm and 90nm
- Enables students to master AMS/Custom design with the Synopsys custom implementation tool suite

- Includes:

Technology Files

Parasitic Extraction Files

Symbol Library and Python PCells

Embedded Memories

Physical Verification Files

HSPICE Models

Callback Scripts

Setup Files

- Used by Synopsys for:

Curricula Development

To support development of laboratory works and course projects.

Customer Education

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Application Consultants

To develop and test sample designs and Reference Methodology scripts.



# Synopsys Generic Memory Compiler

- Configurable software that automatically generates static RAM circuits of different types and sizes with all required deliverables
- Generate custom memory instances for educational ICs
- Designed for use with Synopsys EDKs and EDA tools
- Optimized for the Synopsys Digital Design Flow
- Supports multiple technologies (90nm, 32/28nm, etc.)

## User interface

- Command line
- GUI

## Supported memory types

- 1 port SRAM
- 2 port SRAM
- 1 port Low Power SRAM
- 2 port Low Power SRAM

*“Using the Synopsys Generic Memory Compiler in our complex processor for DSP application was a **great time-saving tool**. It helped the students generate the SRAM they wanted in a snap, saving them critical time to concentrate on the rest of the complex design.”*

***Dr. Maged Ghoneima, American University in Cairo***

# Thank You

Synopsys Academic & Research Alliances (SARA) Taiwan

Contact us  [tw-up@synopsys.com](mailto:tw-up@synopsys.com)  [Global Home Page](#)  [TW Home Page](#)